CLAIM AMENDMENTS

1. (Currently Amended) A semiconductor device comprising:
a semiconductor substrate having at least one DRAM region and one logic region;
a resistor group including a plurality of resistors located in said logic region;
a metal interconnection layer opposite said resistor grouping said logic region; and
a ~~metallic~~ layer including a metal disposed between said resistor group and said metal interconnection layer in said logic region as a shielding layer and partially disposed within said DRAM region.

2. (Currently Amended) The semiconductor device according to claim 1, wherein said ~~metallic~~ layer including a metal is a bit line layer in said DRAM region.

3. (Currently Amended) The semiconductor device according to claim 1, comprising a stacked capacitor in said DRAM region ~~and~~, said stacked capacitor including a lower capacitor electrode layer, a dielectric film, and an upper capacitor electrode layer, said upper capacitor electrode layer being part of said ~~metallic~~ layer including a metal.

4. (Previously Presented) The semiconductor device according to claim 1, wherein said shielding layer has a fixed potential.

5. (Currently Amended) A semiconductor device comprising:
a semiconductor substrate having at least one DRAM region and one logic region;
a signal interconnection layer in said logic region;
a metal interconnection layer in said logic region; and
a ~~metallic~~ first layer including a metal, located ~~in said DRAM region and said logic region and located on one side of~~ between said signal interconnection layer~~, with respect to~~ and said ~~semiconductor substrate,~~ metal interconnection as a first shielding layer in said logic region.

6. (Currently Amended) The semiconductor device according to claim 5, wherein said ~~metallic~~ signal interconnection layer is common to a gate electrode layer in said DRAM region.

7. (Currently Amended) The semiconductor device according to claim 5, wherein said ~~metallic~~ signal interconnection layer is common to a bit line layer in said DRAM region.

8. (Currently Amended) The semiconductor device according to claim 5, comprising stacked capacitor in said DRAM region ~~and~~ said stacked capacitor including a lower capacitor electrode layer, a dielectric film, and an upper capacitor electrode layer, said upper capacitor electrode layer in said DRAM region being part of said ~~metallic~~ first layer including a metal.

9. (Currently Amended) The semiconductor device according to claim 5, wherein said ~~shielding~~ first layer including a metal has a fixed potential.

10. (Currently Amended) A method of fabricating a semiconductor device having at least one DRAM region and one logic region and having a resistor group in said logic region, the method comprising:

forming a resistor group in said logic region;

forming a ~~metallic~~ layer including a metal as a shielding layer in said logic region and in said DRAM region; and

forming a metal interconnection layer opposite a portion of said logic region where said resistor group is located.

11. (Currently Amende) The method according to claim 10, wherein said ~~metallic~~ layer including a metal is a bit line layer in said DRAM region.

12. (Currently Amended) The method according to claim 10, further comprising forming a stacked capacitor having a lower capacitor electrode layer, a dielectric film, and an upper capacitor electrode layer in said DRAM region, wherein said upper capacitor electrode layer is part of said ~~metallic~~ layer including a metal.

13. (Previously Presented) The method according to claim 10, further comprising fixing potential of said shielding layer.

14. (Currently Amended) A method of fabricating a semiconductor device having at least one DRAM region and one logic region and having a signal interconnection layer in said logic region, the method comprising:

forming a first ~~metallic~~ layer including a metal as a first shielding layer in said logic region and in said DRAM region;

forming a signal interconnection layer in said logic region opposite said first shielding layer; and

forming a second ~~metallic~~ layer including a metal as a second shielding layer opposite said signal interconnection layer in said logic region and in said DRAM region.

15. (Currently Amended) The method according to claim 14, wherein one of said first and second ~~metallic~~ layers including a metal is a gate electrode layer in said DRAM region.

16 (Cancelled)

17. (Currently Amended) The method according to claim 14, further comprising forming a stacked capacitor having a lower capacitor electrode layer, a dielectric film, and an upper capacitor electrode layer in said DRAM region, wherein said upper capacitor electrode layer in said DRAM region is part of said second ~~metallic~~ layer including a metal.

18. (Previously Presented) The method according to claim 14, further comprising fixing potential of one of said first and second shielding layers.

19. (New) The semiconductor device according to claim 5, comprising a second layer including a metal, located between said signal interconnection layer and said semiconductor substrate, as a second shielding layer in said logic region.

20. (New) The semiconductor device according to claim 19, wherein said second layer including a metal is common to a gate electrode layer in said DRAM region.